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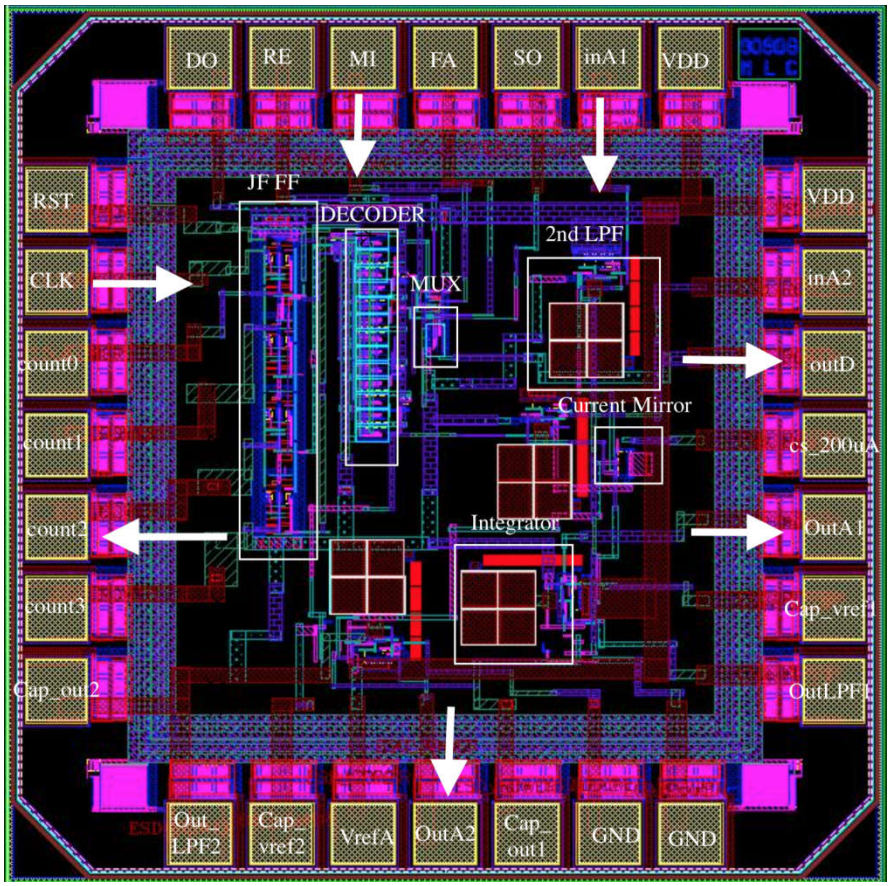
ADVANCED VLSI COURSE IN PHYSICAL DESIGN

Course covers all advanced topics as prescribed by industry requirements



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COURSE SYLLABUS

In this course we use 180nm, 90nm, 45nm and 28nm technology nodes.

All modules are covered in details from basic to advanced topics with practical implementations.

Tools used: **Cadence Encounter and Synopsys DC**

Lab Access: **VPN enabled Tool Servers access**

Module-1: Introduction to VLSI Digital Design

Overview of Digital design methodology, Representations of Digital Design and understanding of digital systems, logic gates, combinational and sequential logic. Review HDL's and RTL implementation of digital logic systems.

Module-2: Semiconductor technologies and CMOS fundamentals

Introduction to semiconductor technologies, logic gates, Review CMOS basics, CMOS digital design concepts. Understanding CMOS process parameters and characterization of logic gates.

Module-3: ASIC design flow and design planning

Overview of ASIC/SOC design flow, Digital Design Concepts and Physical Design flow setup. Review of ASIC fundamentals & fabrication methodologies.

Module-4: ADVANCED DIGITAL DESIGN

a) Introduction to digital design
b) Number representation, complements and Boolean logic
c) Basic logic gates and logic functions
d) Optimization techniques for logic functions
e) Design of combinational circuits.
f) Implementation and analysis of combinational circuits like, adders, comparator, multiplier etc.
g) Design of synchronous sequential circuits.
h) Implementation and analysis of sequential circuits Flip-Flops, registers, counters, and simple processor
i) Design of Asynchronous Sequential Circuits
j) Design of Finite State Machines (FSM)
k) Discussion - Special circuits like LFSR, FIFO, barrel shifter etc.
l) Case study – PROTOCOLS LIKE AHB, APB, PCI, UART etc.

Module-5: VERILOG HDL

a) Introduction to Verilog HDL.
b) Gate-Level modeling.
c) Dataflow modeling.
d) Operators.
e) Data types.
f) Modeling timing and delays.
g) Behavioral modeling.
h) Parameters, tasks and functions.
i) Compiler directives.
j) System tasks.
k) File input/output.
l) Switch-level modeling.
m) User Defined Primitives.
n) Design examples – FSM, ALU, RAM, ROM, UART, Traffic light signal.

Module-6: SYNTHESIS – ASIC DESIGN FLOW

a) Introduction to ASIC's and ASIC flows
b) Insight into various ASIC design Architecture
c) Writing RTL for ASIC design flow
d) ASIC Design Flow using Synopsys and cadence Tools
e) Using special digital modules in ASIC design
f) Static RAM and Dynamic RAM
g) Clock and Reset managements, power sequencing
h) Clock gating and low power designs
i) Dedicated arithmetic functions

Module 7: DESIGNING STRATEGIES

a) Simulation and synthesis issues.
b) RTL design strategies.
c) Static timing analysis.

Module 8: STATIC TIMING ANALYSIS

a) Introduction to STA
b) Comparison with DTA
c) Timing Path and Constraints
d) Different types of clocks
e) Clock domain and Variations
f) Clock Distribution Networks
g) How to fix timing failure

h) Introductions to timing static and dynamic hazards,
i) Path delay, Gate delay, Metastability states.
j) Sequential timing delays like set-up time, hold time,
k) Maximum frequency, violations, slew, slack.
l) Delay analysis
m) Sequential logic pad to set up,
n) pad to pad,
o) clk to next Reg,
p) Reg to o/p and
q) Reg to Reg. violations wrt sequential circuit.

Module-9: ASIC design standard cell libraries and flow setup

Design data preparation, process technologies and standard cell libraries. Understanding of standard cell technology parameters, netlist generation and technology mapping. Reviewing timing constraints and IO constraints. Low power and low area design concepts.

Module-10: Review synthesis principles and synthesis of design modules

Implementation of RTL design and synthesis, generating netlist and estimating performance of synthesized design. Area/timing report checks, design constraints for synthesis. Efficient synthesis techniques. SDF generation

Module-11: Pre-Layout design partitioning and planning

Design plan for hierarchical and flat design implementation, better partition techniques and flow setup.
Special cells and IO cells usage planning, congestion removal techniques and implementation constraint setup.

Module-12: Design floor planning and power planning

Understanding various floor planning techniques, setting up guidelines for better floor planning and meeting design goals. IO PAD placement planning, power planning. Adding power rings and power mesh.

Module-13: Design Placement

Placement techniques, various optimization techniques to avoid design congestion. Performing timing analysis at various levels of floor planning. Pre and post placement optimization technique, setting up placement goals to meet design placement constraints, fixing placement issues.

Module-14: Clock tree synthesis and timing analysis

Implementation of clock tree in placed design, understanding various aspects of timing parameters like clock setup/hold, skew and latency issues, Adding buffers in clock tree and implementing clock tree. Analyzing timing reports after clock tree synthesis and fixing issues.

Module-15: Routing

Various types of routing, trial route, special route, global routing and detailed routing. Analyzing routed design checking post routed design issues, DRC checks, timing checks, optimization of routing constraints.

Module-16: Detailed timing analysis and optimizations, parasitic extraction

Doing complete path and module based timing analysis, checking timing optimizer reports, identifying failing paths, fixing issues. Extracting capacitor table values for the design. IR drop and electro migration analysis.

Module-17: Post route design checks and signoff

Perform DRC, Logical Equivalence checking, generating detailed timing/power reports, generating power reports. GDS-II generation.

Prerequisites:

With Electronics major subject in B.E/B.Tech/M.E/M.Tech, atleast 60% throughout academic career Basic knowledge in Verilog/VHDL Good knowledge on Digital design Good knowledge on any Microcontroller/Processor architectures Good logical & analytical ability

Admission procedure:

Selection based on written test and personal Interviews for eligible interested Candidates. Syllabus for written test covers Digital logic design, Processor architecture, and Analytical and Logical questions. Please walkin/mail/call us to schedule for written test & personal interview. Outstanding performers will get special concessions in Fees. Working VLSI/Software professionals will get direct admissions.

Grading & Certifications

All the participants who fulfilled course assignments, projects, topic wise exams would be awarded with Course completion Certification

Placement Assistance

All the eligible candidates who have fulfilled requirements of the course will be given 100% placement assistance.

Duration:

6 months full time regular weekly & weekend batches

Course Fees:

Rs: 90,000/-