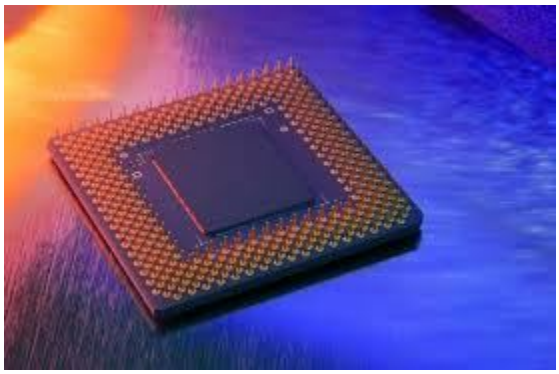
PG DIPLOMA COURSE
IN
VLSI FRONT END DESIGN

An Initiative by Industry Experts
with
qualification from IITs and IISCs



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COURSE SYLLABUS

MODULE 1: INTRODUCTION TO VLSI

1. VLSI DESIGN FLOW
2. ASIC vs FPGA

MODULE 2: ADVANCED DIGITAL DESIGN

1. Introduction to digital design

2. Number representation, complements and Boolean logic

3. Basic logic gates and logic functions

4. Optimization techniques for logic functions

5. Design of combinational circuits.

6. Implementation and analysis of combinational circuits like, adders, comparator, multiplier etc.

7. Design of synchronous sequential circuits.

8. Implementation and analysis of sequential circuits Flip-Flops, registers, counters, and simple processor

9. Design of Asynchronous Sequential Circuits

10. Design of Finite State Machines (FSM)

11. Discussion - Special circuits like LFSR, FIFO, barrel shifter etc.

12. Case study – PROTOCOLS LIKE AHB, APB, PCI, UART etc.

MODULE 3: VERILOG HDL

1. Introduction to Verilog HDL.

2. Gate-Level modeling.

3. Dataflow modeling.

4. Operators.

5. Data types.

6. Modeling timing and delays.

7. Behavioral modeling.

8. Parameters, tasks and functions.

9. Compiler directives.

10. System tasks.

11. File input/output.

12. Switch-level modeling.

13. User Defined Primitives.

14. Design examples – FSM, ALU, RAM, ROM, UART, Traffic light signal.

MODULE 4: SYNTHESIS – FPGA DESIGN FLOW

1. Introduction to FPGAs and FPGA kits

2. Insight into FPGA Architecture

3. Writing RTL for FPGA flow

4. FPGA Design Flow using Xilinx FPGA Kit and Xilinx Tools

5. Using special FPGA Resources in design

a. Block RAM

b. DCM (Digital Clock Manager)

c. Dedicated arithmetic functions

6. FPGA kit interfacing and configuration

a. SSLED

b. PS2 Keyboard

MODULE 5: DESIGNING STRATEGIES

1. Simulation and sythesis issues.
2. RTL design strategies.
3. Static timing analysis.

MODULE 6: STATIC TIMING ANALYSIS

1. Introduction to STA
2. Comparison with DTA
3. Timing Path and Constraints
4. Different types of clocks
5. Clock domain and Variations
6. Clock Distribution Networks
7. How to fix timing failure
8. Introductions to timing static and dynamic hazards,
9. Path delay, Gate delay, Metastability states.
10. Sequential timing delays like set-up time, hold time,
11. Maximum frequency, violations, slew, slack.
12. Delay analysis

12.1 Sequential logic pad to set up,

12.2 pad to pad,

12.3 clk to next Reg,

12.4 Reg to o/p and

12.5 Reg to Reg. violations wrt sequential circuit.

Prerequisites

- With Electronics major subject in B.E/B.Tech/M.E/M.Tech, atleast 60% throughout academic career
- Basic knowledge in Verilog/VHDL
- Good knowledge on Digital design
- Good knowledge on any Microcontroller/Processor architectures
- Good logical & analytical ability

Admission Procedure

Selection based on written test and personal Interviews for eligible interested Candidates. Syllabus for written test covers Digital logic design, Processor architecture, and Analytical and Logical questions.

Please walkin/mail/call us to schedule for written test & personal interview. Outstanding performers will get special concessions in Fees.

Working VLSI/Software professionals will get direct admissions.

Grading & Certifications

All the participants who fulfilled course assignments, projects, topic wise exams would be awarded with **Course completion Certification**

Placement Assistance

All the eligible candidates who have fulfilled requirements of the course will be given 100% placement assistance.

Course Dates & Duration:

- Full time regular batches
- Duration: 10 Weeks
- Weekly and Weekend Batches
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Course Fees:
25,000/-

EDA TOOLS

Our labs are equipped with State-of-the-art Synopsys tools, Mentor Graphics EDA Tools, Windows/Linux based Open-Source EDA tools and demo versions of some industry tools.

- VCS Synopsys compiler
- Modelsim
- Xilinx ISE for FPGA flow
- MATLAB