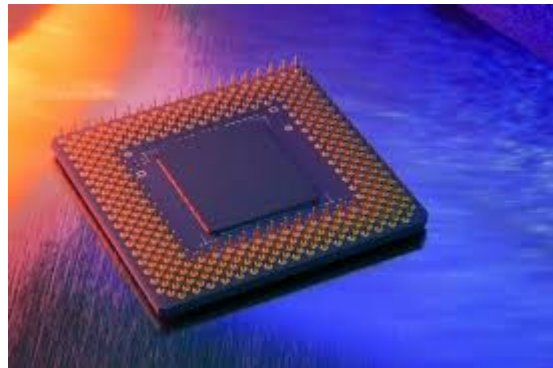


**PG DIPLOMA COURSE
IN
VERIFICATION USING SYSTEMVERILOG**

An Initiative by Industry Experts

With

Qualification from IITs and IISCs



NEOSCHIP SEMICONDUCTORS

3rd Floor, Sai Durga Enclave, 1099/833-1, Near Citrus Hotel, Marathahalli-Sarjapur
Outer Ring Rd, Bellandur, Bengaluru, Karnataka 560103

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Verification Using SystemVerilog

What is SystemVerilog?

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented paradigm features. There are also considerable improvements in the usability of Verilog for RTL design.

Overview

NEOSCHIP's *Verification Using SystemVerilog* course gives you an in-depth introduction to the main enhancements that SystemVerilog offers for testbench development, discussing the benefits and issues with the new features. It also demonstrates how verification is more efficiently and effectively done using SystemVerilog constructs. The course explores in depth verification enhancements such as object-oriented design, constraint random generation, and functional coverage.

Objectives

- To explore the new features of SystemVerilog for verification and demonstrate the improvements in verification environment efficiency from their use.
- To explain key features for verification, such as classes, OOP, randomization, and functional coverage and illustrate how to exploit these features for more efficient verification and testbench development.

Duration

Two and half Months.

Prerequisites

Attendees must be familiar with Verilog and ideally, but not essentially, Verilog2001. No prior knowledge of SystemVerilog is required. If you have queries on these prerequisites, please contact NEOSCHIP.

Contact Address

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Table of Contents

Module 1

1.1 Introduction to Verification Languages

Advanced Verilog Concepts.

- Constant Functions.
- Enhanced Operators.
- Re-entrant tasks and Recursive Functions.
- FILE I/O.
- Common Compiler Directives.
- Enhanced condition compilation.
- Attributes.
- Enhanced Invocation Option Tests.
- New Timing Constraint Checks.
- Verilog Configurations.
- Verilog Generate.

1.1.1 Verilog PLI.

1.1.2 HVL Based verification.

1.2 Verification Tools

- Linting Tools.
- Simulators.
- Waveform Viewers.
- Source Debugging Tools.
- Code Coverage Tools.
- Functional/Assertion Coverage Tools.

1.3 Verification Process in ASIC Flow

1.3.1 Functional Verification Process.

- Test Plan Development.
- TestBench Development
- Testcase Development.
- Behavioral Models Development.
- BFM's Developments.
- Monitors Development.
- Checker Development.
- Functional group & Assert group Development using OVL & SVA.
- Module/Block/Chip Level Verification.
- Coverage driven Random Verification.
- Verification Metric Analysis (Code & Function coverage analysis).

1.4 Timing Verification Process.

- Zero-Delay Gate-Level Verification.
- SDF-Annotated Gate-Level Verification.
- ❖ Timing Verification Process.

- ❖ Introduction to Formal Verification.
- ❖ Introduction Power-Aware Verification.
- ❖ Introduction to co-simulation verification.
- ❖ Introduction to AMS Verification.
- ❖ Introduction to Physical Verification.

1.5 Test-Bench Automation

- a) Introduction to Scripting using Perl.
- b) Linux/Unix Utilities.
 - FTP.
 - Telnet.
- c) Version Management.
- d) Bug Tracking.

Module 2

1.1. Introduction to SystemVerilog

- Language evolution
- SV Design
- SV Assertions
- SV testbench
- DPI
- API

1.2. Abstract modeling constructs

- Data types, type checking, type cast
- Structure and union
- Packages
- Enhanced always, case/if... else, loop, flow
- Operators

1.3. Arrays and its operators

1.4. SV scheduling semantics

1.5. DUT description

1.6. Interface

- Grouping signals
- Modport
- Clocking block, skews
- Tasks, functions
- Transaction Level Modeling (TLM)

1.7. Class

- OOP
- cast
- inheritance
- polymorphism
- parameterization
- new constructor
- Automatic garbage collection
- Virtual interface
- task and function
 - automatic and static
 - void
 - extern
 - Argument pass by value/reference

1.8. Program construct

1.9. Final block

1.10. Enhanced Concurrency modeling

- Threads – variants of fork .. join
- Disable fork, terminate

1.11. Inter process communication

- semaphore
- mailboxes
- queues

Module 3

2.1 Random vs. directed testing

2.2 Need for random testing

- Constraints in SVTB
- Class constraint
- Randomize success / fail
- Inheritance
- Randomize.with()
- Distribution
- Function calls in constraints
- Array constraints
- Pre / post randomize

2.3. Functional coverage

- Motivation
- Introduction
- Types of coverage
- Functional coverage process
- Covergroup
- Coverpoint
- Concept of binning
- Cross
- Sampling event

2.4 . DPI

- Import
- Export
- Context

2.5. DPI vs. VPI/PLI

Module 4

Industry standard project: (Select any one)

- AHB Master/slave
- AXI Master/Slave
- AHB-I2C
- AHB Uart
- AHB Memory controller.
- Microcontrollers/DSP processors
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Prerequisites

- With Electronics major subject in B.E/B.Tech/M.E/M.Tech, atleast 60% throughout academic career
- Basic knowledge in Verilog/VHDL
- Good knowledge on Digital design
- Good knowledge on any Microcontroller/Processor architectures
- Good logical & analytical ability

Admission Procedure

Selection based on written test and personal Interviews for eligible interested Candidates. Syllabus for written test covers Digital logic design, Processor architecture, and Analytical and Logical questions.

Please walkin/mail/call us to schedule for written test & personal interview. Outstanding performers will get special concessions in Fees.

Working VLSI/Software professionals will get direct admissions.

Grading & Certifications

All the participants who fulfilled course assignments, projects, topic wise exams would be awarded with **Course completion Certification**

Placement Assistance

All the eligible candidates who have fulfilled requirements of the course will be given 100% placement assistance.

Course Dates & Duration:

- Full time regular batches
- Duration: 2 ½ months
- Weekly and Weekend Batches
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Course Fees:

29,000/- plus taxes